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1. **Partially-parallel LDPC decoder based on high-efficiency message-passing algorithm**
   Shimizu, K.; Ishikawa, T.; Togawa, N.; Ikenaga, T.; Goto, S.;
   Computer Design, 2005. Proceedings. 2005 International Conference on
   2-5 Oct. 2005 Page(s):503 - 510
   IEEE CNF

2. **A 8-bit MCU design using a four-pipeline architecture**
   Qing-Lan Lv; Ping Li;
   Communications, Circuits and Systems and West Sino Expositions, IEEE 2002 International Conference on
   Volume 2, 29 June-1 July 2002 Page(s):1462 - 1465 vol.2
   IEEE CNF

3. **An architecture for multiresolution, focal, image analysis**
   Burt, P.J.; van der Wal, G.;
   Pattern Recognition, 1990. Proceedings., 10th International Conference on
   Volume ii, 16-21 June 1990 Page(s):305 - 311 vol.2
   IEEE CNF

4. **A triangular systolic array for the discrete-time deconvolution**
   Hussain, M.G.M.; Jaragh, M.;
   Circuits and Systems, IEEE Transactions on
   Volume 36, Issue 4, April 1989 Page(s):622 - 628
   IEEE JNL

5. **A programmable concurrent video signal processor**
   Chih-Chin Chen; Chein-Wei Jen;
   Image Processing, 1996. Proceedings., International Conference on
   Volume 1, 16-19 Sept. 1996 Page(s):1039 - 1042 vol.2
   IEEE CNF

6. **Design and implementation of the control structure of the PAPRICA-3 processor**
   Gregoretti, F.; Intini, F.; Lavagno, L.; Passerone, R.; Reyneri, L.M.;
   Parallel and Distributed Processing, 1996. PDP '96. Proceedings of the Fourth Euromicro Workshop on
   24-26 Jan. 1996 Page(s):290 - 296
   IEEE CNF

7. **A pyramid-based front-end processor for dynamic vision applications**
   Burt, P.J.;
   Proceedings of the IEEE
   Volume 90, Issue 7, July 2002 Page(s):1188 - 1200
   IEEE JNL

8. **Fast Fourier transform processor based on low-power and area-efficient algorithm**
   Jung-yeol Oh; Myoung-seob Lim;
   Advanced System Integrated Circuits 2004. Proceedings of 2004 IEEE Asia-Pacific Conference on
   4-5 Aug. 2004 Page(s):198 - 201
   IEEE CNF

9. **An embedded processor core for consumer appliances with 2.8GFLOPS and 36M polygons/s FPU**
   Arakawa, F.; Yoshinaga, T.; Hayashi, T.; Kiyoshige, Y.; Okada, T.; Nishibori, M.; Hiraoka, T.; Ozawa, M.; Kodama, T.; Irita, T.; Kamei, T.; Ishikawa, M.; Nitta, Y.; Nishii, O.; Hattori, T.;
   Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International
   15-19 Feb. 2004 Page(s):334 - 531 Vol.1

IEEE CNF

10. **High performance single chip dataflow processor**
Kuru, G.;
ASIC Conference and Exhibit, 1995., Proceedings of the Eighth Annual IEEE International
18-22 Sept. 1995 Page(s):346 - 349

IEEE CNF

11. **The bit-serial systolic back-projection engine (BSSBPE)**
Bayford, R.;
Application Specific Array Processors, 1990. Proceedings of the International Conference on
5-7 Sept. 1990 Page(s):43 - 54

IEEE CNF

12. **Video composition methods and their semantics**
Lin, H.-D.; Messerschmitt, D.G.;
Acoustics, Speech, and Signal Processing, 1991. ICASSP-91., 1991 International Conference on
14-17 April 1991 Page(s):2833 - 2836 vol.4

IEEE CNF

13. **An advanced dataflow processor architecture based on a multiple input node concept**
Kuru, G.; Deshmukh, R.G.;
Southeastcon '93, Proceedings., IEEE
4-7 April 1993 Page(s):8 p.

IEEE CNF

14. **Designing pipeline FFT processor for OFDM (de)modulation**
Shousheng He; Torkelson, M.;
Signals, Systems, and Electronics, 1998. ISSSE 98. 1998 URSI International Symposium on
29 Sept.-2 Oct. 1998 Page(s):257 - 262

IEEE CNF

15. **A highly efficient AES cipher chip**
Chih-Pin Su; Tsung-Fu Lin; Chih-Tsun Huang; Cheng-Wen Wu;
Design Automation Conference, 2003. Proceedings of the ASP-DAC 2003. Asia and South Pacific
21-24 Jan. 2003 Page(s):561 - 562

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10207829	Not Issued	61	07/31/2002	Method for improving instruction selection efficiency in a DSP/RISC compiler	KU, SHAN-CHYUN
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